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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,996	07/11/2003	Hiromi Ogasawara	2003-0912A	2779

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EXAMINER	
DOLAN, JENNIFER M	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,996	OGASAWARA ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/11/03, 2/10/04, 4/27/04*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, and 9-13 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2003/0003707 to Yamaha.

Regarding claims 1 and 3, Yamaha discloses a method for manufacturing an element having a substrate (10), a lower wiring (20), an upper wiring (32), a via-hole connecting the lower wiring to the upper wiring (figures 5-9), and a W material filled in the via-hole (paragraphs 0101-0111), comprising: forming the lower wiring layer on top of the substrate (paragraph 0081); forming the via-hole to extend upwardly from the lower wiring layer (paragraphs 0082-0087); feeding a fluorine compound gas having a reducing function into the via-hole, the gas including WF_6 (paragraph 0101); forming a W nucleus in the via-hole (paragraphs 0101-0105); filling the via-hole with W (paragraphs 0106-0111); and forming the upper wiring layer (paragraph 0120).

Regarding claim 9, Yamaha discloses that the filling of the via hole with W is performed by CVD (paragraphs 0015, 0101-0111).

Regarding claim 10, Yamaha discloses that the forming of a W nucleus includes using SiH_4 and WF_6 (paragraphs 0101-0102).

Regarding claim 11, Yamaha discloses forming a first insulation layer (12) between the substrate and the lower wiring layer (paragraph 0066; figure 11).

Regarding claim 12, Yamaha discloses forming a second insulation layer (22) between the lower and upper wiring layers, wherein the via hole extends into the second insulation layer (figure 11; paragraph 0082).

Regarding claim 13, Yamaha discloses performing a sputtering process (paragraph 0088) and forming an adhesive layer (24) on the via hole (paragraph 0088; figure 6) between the forming of the via-hole (figure 5) and the feeding of the fluorine compound (figure 7).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4-8, and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha in view of U.S. Patent No. 5,498,768 to Nishitani et al.

Regarding claims 2, 4-8, and 19, Yamaha discloses a method for manufacturing an element having a substrate (10), a lower wiring (20), an upper wiring (32), a via-hole connecting the lower wiring to the upper wiring (figures 5-9), and a W material filled in the via-hole (paragraphs 0101-0111), comprising: forming the lower wiring layer on top of the substrate

(paragraph 0081); forming the via-hole to extend upwardly from the lower wiring layer (paragraphs 0082-0087); feeding a fluorine compound gas with a reducing function into the via-hole to form a W nucleus in the via-hole (paragraphs 0101-0105); filling the via-hole with W (paragraphs 0106-0111); and forming the upper wiring layer (paragraph 0120).

Yamaha fails to disclose feeding a fluorine compound gas into the vias hole to clean the via hole.

Nishitani discloses applying a fluorine compound gas into the via-hole to clean the via-hole before W deposition (column 5, lines 1-32; column 6, lines 1-18), the compound gas including SiF_4, NF_3 or WF_6 (column 5, lines 1-32; column 6, lines 1-18) in which part of a nucleus is formed (figures 3 and 6). The usage of SiF_4 will automatically form an Si nucleus layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Yamaha, such that a gas including a fluorine compound gas having a cleaning function is applied to the via-hole, as suggested by Nishitani. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a fluorine compound gas with a cleaning function, in order to remove oxide films formed in the via hole, and thus improve contact resistance (see Nishitani, column 2, lines 10-30; column 4, lines 1-50; column 1, lines 1-32; column 6, lines 35-48).

Regarding claim 14, Yamaha discloses that the filling of the via hole with W is performed by CVD (paragraphs 0015, 0101-0111).

Regarding claim 15, Yamaha discloses that the forming of a W nucleus includes using SiH_4 and WF_6 (paragraphs 0101-0102).

Regarding claim 16, Yamaha discloses forming a first insulation layer (12) between the substrate and the lower wiring layer (paragraph 0066; figure 11).

Regarding claim 17, Yamaha discloses forming a second insulation layer (22) between the lower and upper wiring layers, wherein the via hole extends into the second insulation layer (figure 11; paragraph 0082).

Regarding claims 18 and 20, Yamaha discloses performing a sputtering process (paragraph 0088) and forming an adhesive layer (24) on the via hole (paragraph 0088; figure 6) between the forming of the via-hole (figure 5) and the feeding of the fluorine compound (figure 7).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. JP 06-268077 to Nakano discloses forming a W plug using WF_6/SiH_4, followed by WF_6/H_2, and a final WF_6/SiH_4 deposition.

b. U.S. Patent No. 5,804,249 to Sukharev et al. discloses using WF_6 to fill a via.

c. U.S. Patent No. 5,082,413 to Fujita et al. discloses forming a W plug by depositing a polysilicon seed, and reacting WF_6 with the polysilicon.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800